IN THE SPECIFICATION:

Please amend the specification pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked up" version pursuant to 1.121):

~~Each register access path 12, 14 carries three addresses from the accessing unit, two~~ source addresses SRC1, SRC2 and a destination address DST. In the case of data processing operations, the source addresses SRC1, SRC2 define registers in the register files 10,11 which hold source operands for processing by the data processing unit. The destination address DST identifies a destination register into which a result of data processing will be placed. The operands and results are conveyed between the register file 10 or 11 and the respective data processing unit via the access paths 12, 14. In the case of load/store operations, the instruction formats allow memory access addresses A_x, A_y to be formulated from data values held in the registers as described in our copending application [(PWF Ref:)] (GB-9916566.4, entitled An Instruction Set for a Computer). The load/store units access a common address space in the form of a data memory 16 via a dual ported data cache DCACHE 15. For this purpose, each load/store unit has a 64 bit data bus Dx,Dy ~~and a 64 bit address bus Ax,Ay.~~

IN THE CLAIMS:

Please amend the claims pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked up" version pursuant to 1.121):

Cancel claim 13.